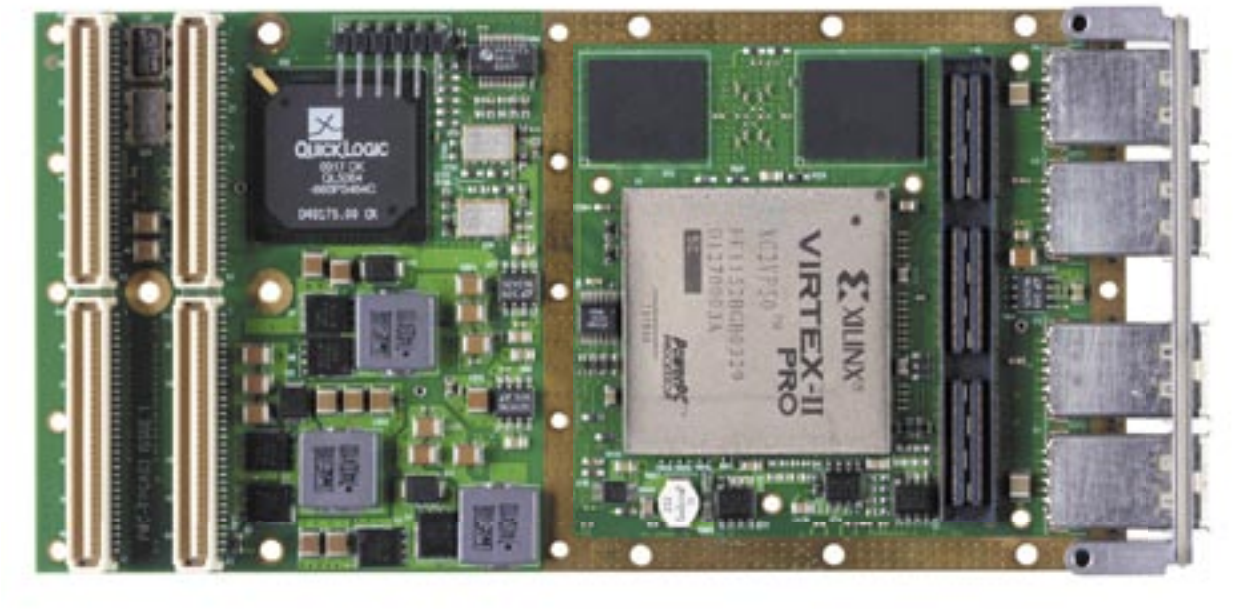
PMC-FPGA03

Xilinx Virtex-II Pro FPGA PMC



Features

Xilinx XC2VP50 Virtex-II Pro™ FPGA

RocketIO: 4 front-panel connections + optional 4 connections to PMC user I/O

138 front panel signal lines + 64 PMC user I/O signal lines

Modular I/O system supporting standards such as LVDS and custom I/O

64-bit/66MHz master/slave PCI interface

2x banks DDR SDRAM (64Mbytes per bank)

3x banks QDR-II SRAM(up to 8Mx18-bit per bank)

4Mbytes Flash Memory

Rugged, conduction-cooled build variants

The PMC-FPGA03 is a Xilinx Virtex-II Pro FPGA based PMC module designed for commercial/ air-cooled and rugged/conduction-cooled build environments where performance counts. To maintain the data throughput of a PMC-FPGA, a range of flexible data I/O options are available either through the front panel (via adaptor modules) or through the PMC's user I/O connector (including Gbps capable RocketIO).

Key applications for the PMC-FPGA03 include realtime imaging, radar and telecommunications.

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FPGA

The heart of the PMC-FPGA03 is a Xilinx Virtex-II Pro XC2VP50 FPGA (in either -5 or -6 speed grade).

Two key features of the Xilinx Virtex-II Pro family of FPGAs are multi-channel Gbps communications (RocketIOs) and embedded PowerPC 405 processors. The PowerPC CPUs can be used for such tasks as protocol stack handling; these are unallocated and free for the user to use.

Flexible Digital I/O

Adaptable digital I/O is a major factor in determining how easy it is to integrate a processing element into a systems environment. With this in mind, the PMC-FPGA03 supports a range of digital I/O options including switch fabric serial comms, LVDS, FPDP and custom interfaces.

The front panel I/O is routed through a 0.5mm pitch, high speed socket. The FPGA is used to control I/O protocols and timings, allowing connection to be made through a simple, low-cost adapter module that provides the standard connectors expected by the I/O scheme being used. 5V, 3.3V and 2.5V power is supplied to the front panel module socket, giving great flexibility to those wishing to design their own modules.

The FPGA signals are banked: two banks (69 signals each) are routed to the front panel and another bank (64 signals) routed to the PMC user I/O connector. Each bank is independently configurable to 2.5V or 3.3V signaling.

PMC-FPGA03 fitted with one of the LVDS I/O module (LVDS-MOD3) options

RocketIO

As an alternative to parallel digital I/O, the PMC-FPGA03 can use high-speed serial communications through the FPGA's RocketIO™ ports. Each of these ports can operate at up to 2.0 Gbps (-5 speed grade) or up to 3.125Gbps when using a -6 speed grade FPGA. Each channel has a separate input and output differential pair.

PMC-FPGA03 fitted with HSSDC2 connectors for 2Gbps front panel RocketIO

RocketIOs can be used either as low-level data 'pipes' or to implement interfaces such as serial RapidIO or Infiniband using firmware IP cores.

Front panel RocketIO uses four Infiniband 1X connectors. Four other RocketIOs are available via the PMC user I/O connector (but at reduced speed).

Note: RocketIOs and digital I/O signals use a common user I/O connector and front panel space, so not all RocketIOs and digital I/Os are available at the same time. See table below for I/O permutations. Standard builds are in blue.

Opt	Front Panel I/O	PMC user I/O (P4)
1	4x RocketIO	4x RocketIO and 28 digital
2	4x RocketIO	64-digital
3	138 digital	64 digital
4	138 digital	4x RocketIO and 28 digital

Memory

The PMC-FPGA03 eases algorithm implementation by supplying the designer with two types of high performance external memory: SDRAM for high capacity and SRAM for fast random access.

SDRAM

Two independent banks of DDR SDRAM (each 64Mbytes) are connected directly to the FPGA and clocked at 125MHz.

QDR SRAM

Three banks of QDR-II SRAM, each with independent port operation to the FPGA are supported, clocked at 125MHz. Each QDR SRAM has the ability to perform read and write operations concurrently and has an aggregate bandwidth of up to 1Gbyte/sec. Transtech supports 1 or 2Mx18-bit banks. The device footprint is capable of taking higher capacity devices as they become available (e.g. 8Mx18-bit).

PCI Interface

The PMC-FPGA03 features a 64-bit/66MHz initiator/target PCI interface and includes full FPGA to PCI interrupts and DMA. The PCI core interface has six FIFOs, four DMA engines, mailbox registers and complex interrupt support. Example VHDL code is provided to allow the developer accelerated access to the built-in resources of the PMC module.

Environmental

The PMC-FPGA03 is available in a number of ruggedized variants; including conduction-cooled variants, hardened against vibration and shock across four levels of ruggedization from the rugged PMC specifications. All build variants are software compatible, meaning that code can be developed on a commercial temperature/air-cooled card with the confidence that it will work on a deployed conduction-cooled card too (NB: the conduction-cooled version has no front panel I/O).

Software

A range of software development tools are available or currently under development for the PMC-FPGA03. These include low level VHDL code, drivers, board support utilities, high-level design tools and IP cores.

Board Support Package

Library firmware, creating standard interfaces between the FPGA and other board hardware, is supplied in the BSP. This has been developed with Xilinx ISE 6.2i logic design tools, so HDL synthesis is with Xilinx synthesis technology (XST). Transtech manuals guide users on transitioning to other synthesis tools such as Synplicity Synplify.

Software development is supported by a board support package (BSP) that includes device drivers, a set of host-based utilities, host application libraries, numerous example programs and full source code to the libraries and device drivers.

The host utilities provide a set of tools to help give oversight of the board architecture, allow for system evaluation, functional testing and configuring of the FPGA.

- bview: Provides a complete display of the installed PMC-FPGA03 hardware including all Xilinx and interface registers as well as Flash and SDRAM memory. This is suitable for detailed debugging.
- bviewd: A remote monitor for non-Microsoft platforms such as VxWorks.
- pfcfg: Allows data files to be copied into the FLASH memory of any Transtech PMC-FPGA product.
- pfprobe: A general purpose system status evaluation tool that is able to probe the system bus for all PMC-FPGA boards. For each card found, it is able to display board information, perform a complete functional test of the board and assess the PCI data transfer bandwidth of the board.

The libraries provide integration support and levels of abstraction for using the PMC-FPGA03 from a host application. They are C++ libraries built using Microsoft Visual C++ for Microsoft Windows NT/2000/XP platforms and the GNU compiler for VxWorks, Linux & LynxOS.

Example programs using these library routines and interfacing with example firmware are included to demonstrate tasks such as setting up DMAs, using the DDR SDRAM and QDR-II SRAM and how the board handles interrupts.

IP Cores

Proven firmware designs for a multitude of algorithms are available from many sources, including Transtech, in the form of intellectual property (IP) cores. See *http://www.transtech-dsp.com* for more information on available cores.

Design Services

Often, FPGA code development, even using standard IP cores requires an amount of engineering development to implement external interfaces and integration of user VHDL code. Call Transtech for information on possible design services to help ease this transition.

I/O Modules

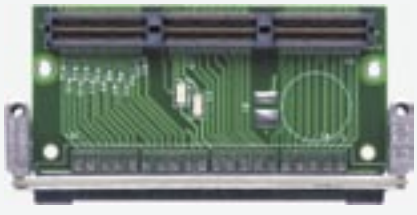
The PMC-FPGA03 is designed to provide a high degree of I/O flexibility including both front panel and PMC P14 based [user] I/O. Front panel I/O has the added benefit of providing I/O modules suitable for a variety of interfaces; the FPGA handles the protocol, the module provides the connector, pin-out and signal conditioning. This makes design and development of new I/O modules simple. Two such modules proved by Transtech DSP are outlined below.

LVDS-MOD3 I/O Module

LVDS I/O Module: LVDS-MOD3

The LVDS-MOD3 is a transition module designed to passively route I/O signals from the PMC-FPGA03 high density connector to a standard 68-way SCSI-3 style front panel connector for ease of connections.

- Up to 32 LVDS signal pairs (18 FPGA bank 0, 14 FPGA bank 1)
- Uses SCSI-II compatible pinout for low cost cabling
- 2.5/3.3V signaling
- Up to 8 (4 pairs) global clock inputs
- 100Ω trace length matched I/O



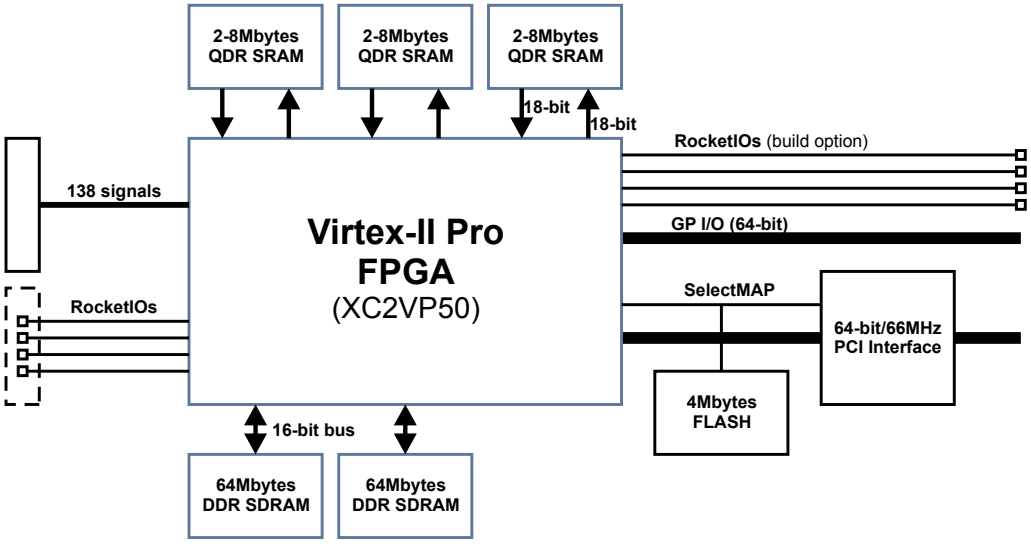
LVDS-MOD4 I/O Module

High Density LVDS I/O Module: LVDS-MOD4

The LVDS-MOD4 is a transition module designed to provide the maximum number of LVDS signals possible. This requires the use of a high-density impedance match connector.

- Up to 132 signals (66 LVDS pairs)
  (66 signals/33 pairs FPGA bank 0, 66 signals/33 pairs FPGA bank 1)
- 100Ω trace length matched I/O
- 2.5/3.3V signaling
- Up to 8 (4 pairs) global clock inputs (two pairs per FPGA bank 0/1)
- AMP/Tyco 767044-4 front panel connector

Block Diagram



Technical Specification

FPGA

Device	Xilinx Virtex-II Pro XC2VP50 (call for other FPGA sizes)
Package	FF1152

Memory

DDR SDRAM	2x 64Mbytes clocked at 125MHz
SRAM	3x 1Mx18-bit or 2Mx18-bit (QDR-II) clocked at 125MHz
FLASH	4Mbytes FPGA boot/configuration Programmable via PMC/PCI interface

PCI

Device	QL5064
Compliance	32/64-bit PCI 2.2 33/66MHz 3.3/5V tolerant Master/slave/DMA
Enhancements	DMA, interrupt support
Bandwidth	>500Mbytes/sec

Input/Output

Front Panel	Samtec QSH-090-01-FDA header (138-bit data/clocks plus power) or 4x RocketIO channels (Molex HSSDC 2)
User I/O (PMC P14)	64-bit data or 28-bit data plus 4x RocketIO channels

Standards

Conforms to	IEEE 1386.1 (PMC module) specification and ANSI/VITA-20-2001 for conduction-cooled PMC

Environmental

	Level 1	Level 2*
Cooling	Air/Convection	Air/Convection
Temperature (Operating)	0°C to 55°C	-10°C to 65°C
Temperature (Storage)	-40°C to 85°C	-40°C to 85°C
Humidity	0 to 95% non-condensing	0 to 100% non-condensing
Vibration (Sine)	na	na
Vibration (Random)	na	0.02 g^2/Hz 20 to 2000 Hz
Shock	na	30 g peak half sine 11 ms
Conformal Coat	No	Yes

	Level 4*
Cooling	Conduction
Temperature (Operating)	-40°C to 75°C
Temperature (Storage)	-55°C to 85°C
Humidity	0 to 100% non-condensing
Vibration (Sine)	10 g peak 15-2000Hz
Vibration (Random)	0.1 g^2/Hz 15-2000Hz
Shock	40 g peak half sine 11 ms
Conformal Coat	Yes

Software Support

Tool chain	Xilinx ISE 6.x XST
Utilities	Flash and FPGA programming (VxWorks and Windows NT/2000)
Library	DMA based host communications

Note: * Call for availability

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